



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,430	10/23/2003	Roger W. Lindsay	400.263US01	8403
27073 7590 11/01/2007 LEFFERT JAY & POLGLAZE, P.A. P.O. BOX 581009 MINNEAPOLIS, MN 55458-1009			EXAMINER LUU, CHUONG A	
			ART UNIT 2818	PAPER NUMBER
			MAIL DATE 11/01/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

514

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/692,430	LINDSAY, ROGER W.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Chuong A. Luu	2818	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 August 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4, 6-28 and 42-62 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9-28 and 42-62 is/are allowed.
- 6) ☒ Claim(s) 1-4 and 8 is/are rejected.
- 7) ☒ Claim(s) 6-7 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-4 and 8 have been considered but are moot in view of the new ground(s) of rejection.

### ***Allowable Subject Matter***

The indicated allowability of claim 5 is withdrawn in view of the newly discovered reference(s) to Li et al. (U.S. 6,771,536). Rejections based on the newly cited reference(s) follow.

### ***Claim Objections***

Claim 7 is objected to because of the following informalities: Claim 7 is depending on claim 5, which is cancelled . Appropriate correction is required.

## **PRIOR ART REJECTIONS**

### **Statutory Basis**

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

### **The Rejections**

Claims 1-4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (U.S. 6,771,536) in view of Chang (U.S. 5,687,118).

L discloses a Non-Volatile memory with

**(1)** forming a source slot and a drain contact region at opposite ends of a NAND string disposed on a substrate of the memory array, the NAND string comprising a plurality of memory cells connected in series between a source select gate and a drain select gate, wherein a portion of the drain contact region is formed directly over the drain select gate and wherein the single mask defines areas for exposing the substrate; forming a source line in the source slot and a drain contact in the drain contact region (see Figure 3);

**(2)** further comprising, before forming the source slot and the drain contact region, forming a dielectric layer on the substrate, the NAND string, and source and drain select gates (see Figure 3);

**(3)** further comprising aligning the drain contact region to a sidewall of the drain select gate (see Figure 3);

**(4)** wherein forming the source slot and the drain contact region comprises removing the dielectric layer from the substrate (see Figure 3);

**(8)** further comprising aligning the source slot to a sidewall of the source select gate (see Figure 3);

Li teaches the above claimed invention except for using a single mask.

However, Chang discloses a memory cell with **(1)**.. using a single mask (see column 12,

lines 49-52). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Li and Chang. Doing so would facilitate the manufacture of the semiconductor device and reduce the manufacturing cost during fabrication of the semiconductor structure.

***Allowable Subject Matter***

Claims 6-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 9-28 and 42-62 are allowed.

The following is an examiner's statement of reasons for allowance: The examiner has reviewed the prior art in light of applicant's claimed invention and finds that the combined claims define over the prior art. The cited prior art does not disclose or suggest a semiconductor memory transistor inter alia the limitations "...forming a drain select gate overlying the substrate and adjacent a drain of a last floating-gate transistor of the plurality of serially-connected floating-gate transistors, a source of the drain select gate coupled to a drain of the last floating-gate transistor; forming a first layer of dielectric material overlying the source select gate, the NAND string, the drain select gate, and exposed surfaces of the substrate adjacent the source and drain select gates; forming a second layer of dielectric material overlying the first layer of dielectric material, wherein the second layer of dielectric material comprises a dielectric material different from the first layer of dielectric material; patterning the second layer of

Art Unit: 2818

dielectric material to expose portions of the first layer of dielectric material adjacent the source select gate, adjacent the drain select gate and overlying the drain select gate to thereby define a source slot and a drain contact region substantially concurrently; removing exposed portions of the first layer of dielectric material adjacent the source select gate and adjacent the drain select gate, thereby exposing portions of the substrate adjacent the source select gate and the drain select; forming a first layer of conductive material overlying the second layer of dielectric material and in contact with the exposed portions of the substrate; removing an upper portion of the first layer of conductive material to recess it below a surface of the second layer of dielectric material, thereby leaving a first portion of the first layer of conductive material in the source slot and a second portion of the first layer of conductive material in the drain contact region; substantially concurrently forming a source line coupled to the first portion of the first layer of conductive material and a drain contact coupled to the second portion of the first layer of conductive material; forming a third layer of dielectric material overlying the second layer of dielectric material, the source line, and the drain contact; forming a bit line contact through the third layer of dielectric material and coupled to a portion of the drain contact overlying the drain select gate...”

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven H. Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Chuong Anh Luu  
Patent Examiner  
October 26, 2007